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| 10/823,244 | 04/12/2004 | Jing-Horng Gau | JCLA12737 | 4067 |

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J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
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| 3663 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/823,244 | GAU, JING-HORNG | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 3663 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4/18/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Amendment filed 4/18/06 forms the basis for this office action. In said Amendment applicant substantially amended claims 1-9 at least through substantial amendment of independent claim 1.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claims 1-9*** are rejected under 35 U.S.C. 102(b) as being anticipated by Russ et al (US 2003/0047750 A1).

*Russ et al teach* (title, abstract, Figure 2 and [0031]-[0039]) a junction diode, comprising :

a first conductive type (p-type) substrate 203 (i.e., the further limitation of claim 2 is met);

a second conductive type (n-type; i.e., the further limitation of claim 3 is met) embedded region $210_1/206_2/205/208/206_2/210_2$ formed within the first conductive type substrate;

a second conductive type (n-type; hence the further limitation of claim 4 is met) epitaxial (hence the further limitations of claims 5 and 6 are met) well 208, formed within the second conductive type embedded region,

wherein the second conductive type well has a dopant concentration smaller than the second conductive type embedded region (see [0033]), and

the second conductive type embedded region surrounds the second conductive type well (Figure 2);

one first conductive type (p-type) doped region 212, formed in said second conductive type well; and

two second conductive type (n-type; hence the further limitation of claim 8 is met) regions $210_1$ and $210_2$, formed in the second conductive type embedded region beside the first conductive type doped region.

*On claim 9:* the junction diode further comprises a plurality of isolation structures 218 (see [0035]) set between the first conductive type doped region and the second conductive type doped regions.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 10-17*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Russ et al (2003/0047750 A1) in view of Amerasekera (EP 0 822 596 A2).

*Russ et al teach* (title, abstract, Figure 2 and [0031]-[0039]) a junction diode, comprising :

a first conductive type (p-type) substrate 203;

a second conductive type (n-type) embedded region $210_1/206_2/205/208/206_2/210_2$ formed within the first conductive type substrate;

a second conductive type (n-type) epitaxial well 208, formed within the second conductive type embedded region,

wherein the second conductive type well has a dopant concentration smaller than the second conductive type embedded region (see [0033]), and

the second conductive type embedded region surrounds the second conductive type well (Figure 2);

a first conductive type (p-type) doped region 212, formed in said second conductive type well; and

at least two second conductive type (n-type) regions $210_1$ and $210_2$, formed in the second conductive type embedded region beside the first conductive type doped region.

*Russ et al do not necessarily teach* an additional substrate underneath said substrate and of conductivity type opposite to said first conductive type.

*However, it would have been obvious to include said additional substrate in view of Amerasekera,* who, in a patent document drawn to improvements in ESD circuits, hence analogous art, teach the addition of a substrate underneath an active area so as

to produce vertical bipolar structure for additional ESD protection (see Summary of the Invention, columns 1 and 2, and Figures 1a, 1b and 3).

*Motivation* for the adoption in the invention by Russ et al by the additional ESD protection a vertical bipolar structure provides, the invention by Russ et al not having said vertical bipolar structure: because 210, 206 and 205 are all of n-type conductivity, only a limited region vertically underneath 212 would otherwise have said vertical bipolar structure to protect against ESD. Upon interchanging conductivity type nomenclature, combination of said teaching with said invention yields the structure of claim 10, just as adding an additional substrate of a conductivity type opposite to the substrate of Figure 2 in the specification by Applicant yields the junction diode of claim 10 from the junction diode of claim 1: specifically, the junction diode comprising: a first conductive type substrate (n-type substrate following Amerasekera); a second conductive type deep well formed within said first conductive type substrate (the p-type substrate of Russ et al, element 203); a first conductive type well formed within the second conductive type deep well (the n-type region defined by the union of $210_1$ , $206_2$ , 205, 208, $206_2$, and $210_2$); a first conductive type shallow well formed within the first conductive type well (namely: n-type region $206_1/206_2/208/214$), wherein the first conductive type shallow well has a dopant concentration smaller than the first conductive type well (see [0033]); a plurality of first conductive type doped regions formed in the first conductive type well (n-type regions $210_1$, $210_2$); and a plurality of second conductive type doped regions formed in the second conductive type deep well (p-type regions $212_1$, $212_2$) and one second conductive type doped region formed in the

first conductive type shallow well (p-type region 214), wherein the second conductive type doped region formed in the first conductive type shallow well (214) is isolated from the second conductive type deep well (203) by the first conductive type well ($210_1$/2062/205/208/$206_2$/$210_2$).

*On claim 11-16:* the specific selections of conductivity type as limited by these claims merely pertain to the selection of p-type conductivity type as the first conductivity type, and logically following, n-type conductivity as the selection of the second conductive type. Overall interchange of conductivity in the semiconductor device art is without patentable weight unless disclosed to be critical to the invention. In the underlying case, both conductivity types are actually disclosed to be equivalent by Applicant (see specification, paragraph [0012]).

*On claim 17:* the junction diode further comprises a plurality of isolation structures 218 (see [0035]) with each isolation structure set between every pair of first conductive type doped region and second conductive type doped region (regions 212 and 210, respectively; see Figure 2).

***Response to Arguments***

Applicant's arguments filed 4/18/06 have been fully considered but they are not persuasive:

(a) With regard to the arguments in traverse of the rejection of newly amended claims 1-9 now by admission by applicant brought back to those in a previous amendment (see Remarks page 5), namely the amendment filed 7/21/05, examiner offers the following comments in response:

Applicant misunderstands applicant's claim language in his comments in traverse of the rejection over Russ et al (see pages 5-7 of Remarks): "one first conductive type doped region" does not mean "only one conductive type doped region". At least for this reason, arguments in traverse of the rejections under 35 USC 102(b) based on this misunderstanding fail to persuade. Parenthetically, even arguendo, applicant here appears to teach against his own second preferred embodiment, in which there are indeed more than one regions of each of two conductive type regions (Figure 3, elements 308 and 310; see [0029]-[[0034]). Taken as a whole, applicant's invention covers the range of one and more than one of said first conductive type doped region without preference for either one or more than one such region expressed, let alone explained.

For at least all of the above reasons, the rejection of claims 1-9 as being anticipated by Russ et al stands.

(b) With regard to the arguments in traverse of the rejection of claims 10-17, especially applicant's allegation of the examiner's misunderstanding of the language of claim 10, applicant appears to have missed the discussion on pages 5 and 6 in which the examiner explained in detail how the implementation of the teaching by Amerasekera transforms the invention by Russ into the recited claim limitations. Examiner specifically recited all limitations in claim 10 and identified how the combination of Amerasekera with Russ causes said claim limitations to be met starting from those met by Russ et al and recited on page 4 of the previous office action, and

ending with the limitations of the actual claim 10 as recited on pages 5-6 of said previous office action.

Therefore, the arguments in traverse of the rejection under 35 USC 103(a) of claim 10-17 as being unpatentable over Russ et al in view of Amerasekera are in error, and the rejection stands.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
June 24, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER